CLAIMS

What is claimed is:

1. An apparatus comprising:

a first transistor device including first, second, and third terminals;

a second transistor device including first, second, and third terminals;

a first impedance device to couple the second terminal of the second transistor device to the first terminal of the first transistor device; and

a second impedance device to couple the second terminal of the first transistor device to the first terminal of the second transistor device, wherein the first and second impedance devices include capacitive and resistive impedance characteristics.

2. The apparatus of Claim 1, wherein the first and second impedance devices comprise substantially the same capacitive and resistive impedance characteristics.

3. The apparatus of Claim 1, wherein a voltage build-up across the first impedance device extends a voltage peak that can be applied at the first terminal of the first transistor device and maintain an operating second terminal voltage of the second transistor device.

4. The apparatus of Claim 1, wherein a voltage build-up across the second impedance device extends a voltage peak that can be applied at the first terminal of the second transistor device and maintain an operating second terminal voltage of the first transistor device.

5. The apparatus of Claim 1, wherein the first impedance device comprises a resistive element in parallel with a capacitive element.

6. The apparatus of Claim 1, wherein the second impedance device comprises a resistive element in parallel with a capacitive element.

7. The apparatus of Claim 1, wherein a maximum output voltage swing provided between first terminals of the first and second transistor devices is based on the impedance of the first and second impedance devices.

8. The apparatus of Claim 1, further comprising:

a first inductive element to couple the first terminal of the first transistor device to a voltage bias;

a second inductive element to couple the first terminal of the second transistor device to the voltage bias;

a capacitive element to couple the first terminal of the first transistor device to the first terminal of the second transistor device; and

a current source coupled to the third terminals of the first and second transistor devices.

9. A system comprising:

a signal retimer device to regenerate a first signal based on a clock signal, wherein the signal retimer device comprises a clock generator to provide the clock signal and wherein the clock generator comprises:

a first transistor device including first, second, and third terminals,

a second transistor device including first, second, and third terminals,

a first impedance device to couple the second terminal of the second transistor device to the first terminal of the first transistor device, and

a second impedance device to couple the second terminal of the first transistor device to the first terminal of the second transistor device, wherein the first and second impedance devices include capacitive and resistive impedance characteristics, wherein a maximum output voltage swing provided between first terminals of the first and second transistor

devices is based on the impedance of the first and second impedance devices;

a data processor to receive the regenerated first signal; and

an interface device to exchange signals with the data processor.

10. The system of Claim 9, further comprising a XAUI compatible interface to couple the data processor with the interface device.

11. The system of Claim 9, wherein the data processor comprises logic to perform media access control in compliance with IEEE 802.3.

12. The system of Claim 9, wherein the data processor comprises logic to perform optical transport network de-framing in compliance with ITU-T G.709.

13. The system of Claim 9, wherein the data processor comprises logic to perform forward error correction processing in compliance with ITU-T G.975.

14. The system of Claim 9, further comprising a switch fabric coupled to the interface device.

15. The system of Claim 9, further comprising a packet processor coupled to the interface device.